VERTIV.

Technical Note

Multilevel Inverter Topologies for UPS Applications

Abstract

The cost of data center downtime is rising than ever before due to the supreme dependency of many digital applications in the day to day business operations. It is estimated that today's downtime cost of the outage is as high as several thousand dollars per second as compared to several hundred dollars per minute a decade ago. Data center outage can cause huge operational loss that impacts the company's productivity and brand reputation. Thus, it is important to design a supported infrastructure in digital ecosystem with highest uptime and greater agility, which comprises of several critical equipments which need to operate perennially.

An uninterrupted power supply is considered as one of the most critical equipment in the electrical ecosystem of the digital infrastructure. The UPS protects the load from unwanted electrical disruptions and provides uninterrupted quality power for continuity of digital operations. As said earlier, the reliability of these key components is vital to ensure highest level of uptime for the data center facility.

This paper is dedicated to explaining the concepts of different inverter topologies that is used in the design of uninterrupted power supplies. It analyzes the performance of different topologies on basic technical parameters that can describe the conduct of UPS on availability and energy efficiency aspects.

Introduction

UPS systems continue to play a key role in providing the quality power against various line problems. Online double conversion UPS is a preferred solution due to its proven reliability against all types of power disturbances. The working principle of online UPS is depicted in Figure 1.

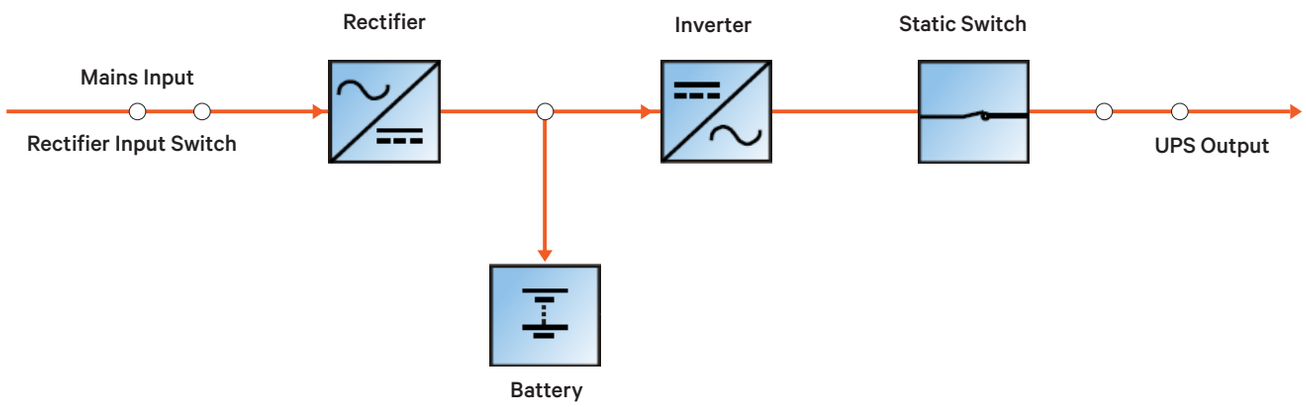

Figure 1 : Online UPS Topology

A double-conversion (Online) UPS provides consistent, clean, and perfect power regardless of the incoming power conditions. The basic function/working principle of online UPS topology is that it converts incoming AC power to DC, and then returns to AC.

During double conversions, the UPS naturally consumes certain amount of power. Therefore, it is essential to minimize the power loss by employing highly efficient technologies without compromising the overall system reliability.

Multi-level topology provides favorable benefits for UPS systems as compared to conventional two-level converters in order to improve the efficiency of double conversion UPS.

Multi-level inverters were initially proposed for high voltage applications to reduce the voltage ratings of power switches. Currently, multi-level converter topology is applied to several low voltage electrical equipment instead of conventional two level inverters, with the aim of reducing voltage distortions and improving the efficiency levels.

Two-level Inverter

The topology of two-level inverter is depicted in Figure 2 (a). This conventional and reliable inverter topology is predominantly used in most of the UPS, Inverters, and other drive applications. In this topology, the voltage stress on each IGBT can be as high as the DC link voltage Vdc. For low-voltage UPS applications (e.g., Vdc = 625 VDC @415 VAC), it employs 1200 V IGBT/diode devices to block the full DC voltage. This topology employs simple PWM techniques & requires moderate amount of LC filters to synthesize pure sinusoidal waveform. It is reliable due to simple power schematic and modulation strategies. However, this topology consumes more power during conversion due to high amount of switching and filter losses.

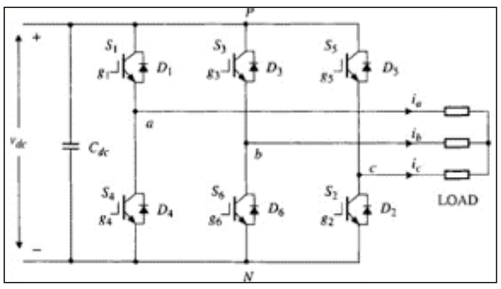

Figure 2(a): Schematic of a Two-level inverter

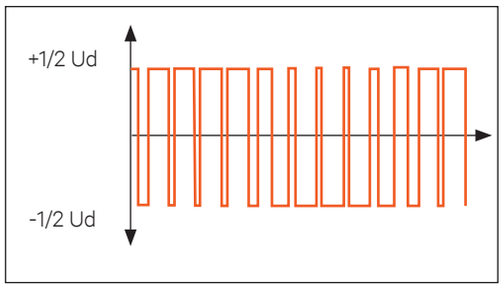

Fig. 2(b) : AC output voltage without filtering

Figure 2

Three-level T-type Inverter

The basic topology of three-level T-type inverter is depicted in Figure 3 (a). The conventional two-level VSC topology is upgraded with an active bidirectional switch to the DC-link midpoint. It is an alternative to more complex three-level topologies such as active neutral point clamped converters or split-inductor converters.

For low-voltage UPS applications (e.g., Vdc = 720 V @ 415 VAC), the high-side and low-side switches (T1 /D1 and T4 /D4) would usually be implemented with 1200 V IGBTs/diodes as the full DC-link voltage has to be blocked. Whereas the bidirectional switches at the DC-link midpoint are implemented with 650 V IGBTs/diodes as half of the DC link voltage has to be blocked. Due to the reduced blocking voltage, the middle switch displays very low switching losses and acceptable conduction losses, although two devices are connected in series.

The three-level T-type inverter basically combines the positive aspects of the two-level inverter such as low conduction losses, small part count and a simple operation principle along with additional advantages like low switching losses and improved output voltage quality.

Apart from the above advantages, the semiconductor losses of the three-level T-type inverter are minimized since it is evenly distributed over several components. Minimized losses result in partial increase in the junction temperature of semiconductor devices, allowing smaller semi-conductor chip sizes to be selected and thus providing higher efficiency and reliability.

Due to the low conduction and switching losses in the three-level T-type inverter, the efficiency is very high especially for medium switching frequency range (8–24 kHz).

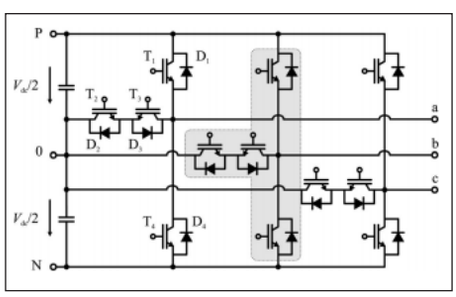

Fig. 3 (a): Schematics of a Three-level T-type inverter

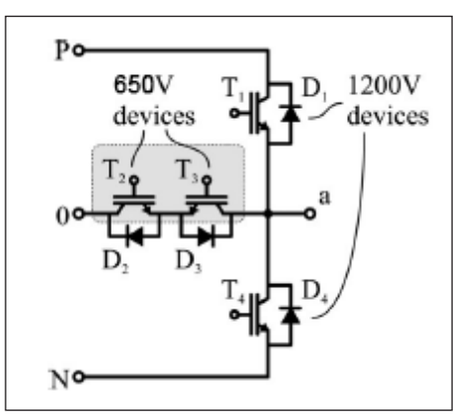

Fig. 3 (b): Schematics of single leg inverter

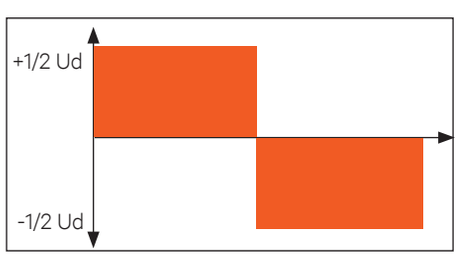

Fig. 3 (c) : AC output voltage without filtering

Figure 3

Four-level Inverter

The basic topology of the four-level inverter is depicted in Figure 4 (a). For low-voltage UPS applications (e.g., Vdc = 750 V @ 415 VAC), each leg of four-level inverter uses six number of IGBTs in which four of them are rated for 600 V and two for 1200 V. Four-level inverter based UPS typically develop a switching voltage of 250 V across IGBTs which results in lower switching losses. However, conduction losses also proportionally increase with increased number of active components. These increased conduction losses can be compensated by the reduction of switching & filter losses. Therefore, the efficiency of three-level t-type and four-level is comparable.

With the appropriate switching frequency coupled with four-level switching, the resulted waveform approaches in the form of a sine-wave. Thus, four-level topology only requires smaller LC for delivering sinusoidal AC output voltage.

But with the increased number of IGBT switches in the four-level inverter, topology demands more complex power circuitry, modulation strategies, and protection circuitry with respect to the three-level T-type inverters. Therefore, four level topology needs to be designed very carefully for the reliable operation.

And on top of above, four-level topology with less voltage stress across IGBTs has allowed the UPS to operate on very high DC bus voltages. The advantage of higher DC voltage entice a wider input voltage range, since the operation of a boost-type PFC rectifier requires DC bus voltage to be above the peak of line voltage. However, the higher DC bus voltage potentially increases the safety operating concerns, therefore, contacting with it directly or through moist objects result in fatal risk, which impacts the overall system reliability.

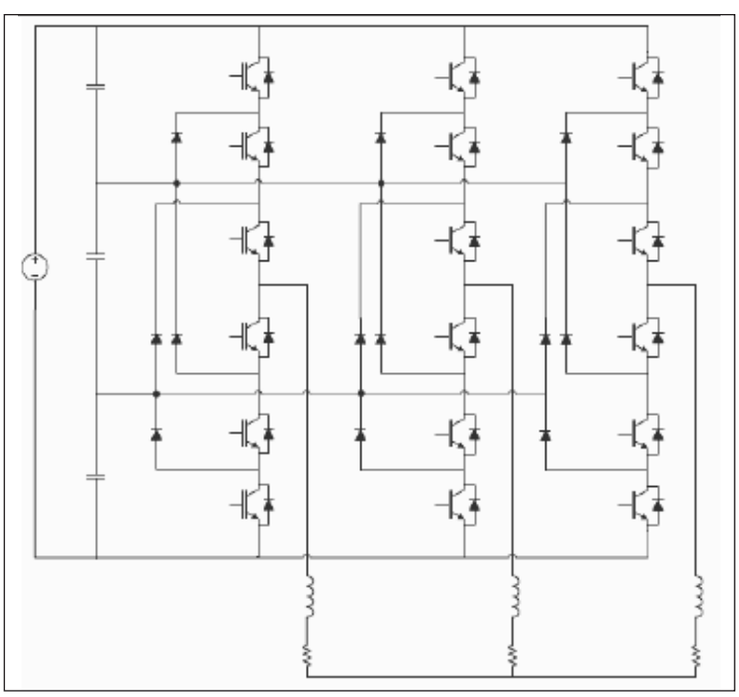

Fig. 4 (a) : Schematic of a four-level neutral point clamped inverter topology

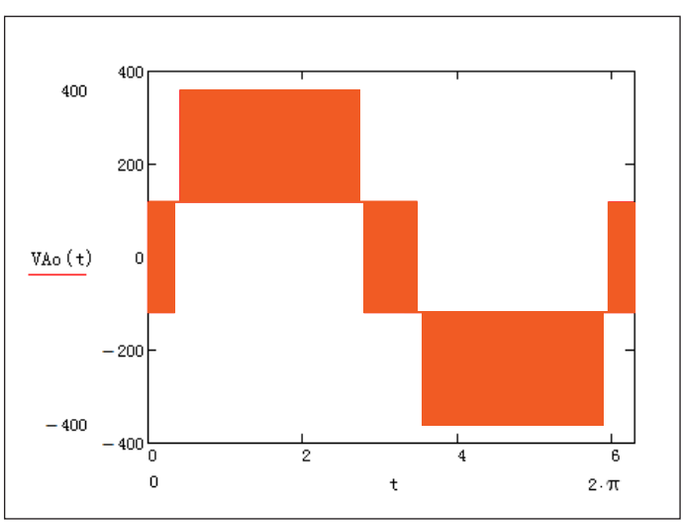

Fig. 4 (b) : AC output voltage without filtering

Figure 4

Five Level Inverter

The basic topology of five level inverter is shown in Figure 5. This topology requires a maximum/greater number of active components (i.e. 12 no of diodes and 8 no of IGBTs), which increases device losses, cost and circuit complexity. Some of the advantages of this topology include the improved output waveform, as it produces nearly sinusoidal output voltage waveforms. Hence the total harmonic distortion is low & the filter needed to smoothen the output voltage is small.

Moreover, the device losses in this topology are higher when compared to 4-level topology. The major challenge with this topology is to balance DC bus voltage. Therefore, this topology is not yet widely implemented for UPS applications due to its circuit complexity and control challenges.

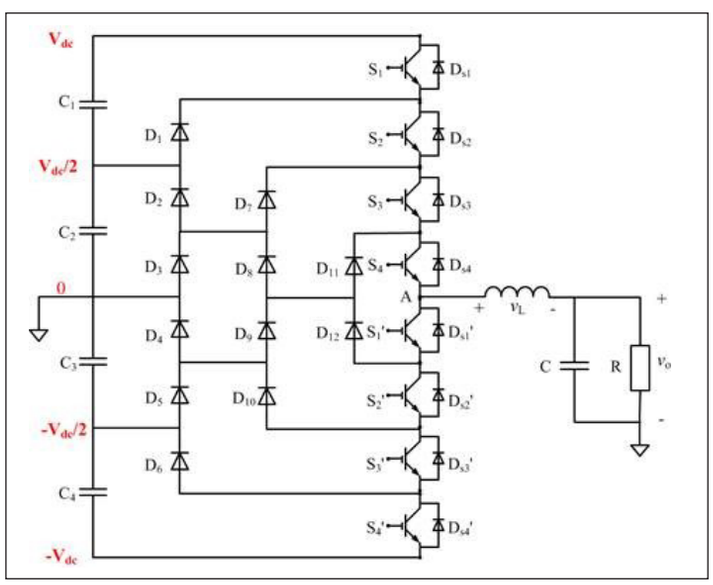

Fig. 5 (a) : Schematic of a five-level diode - clamped inverter topology

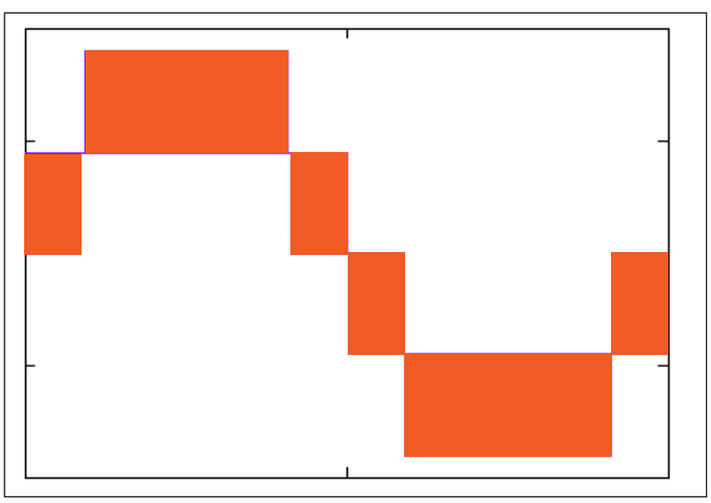

Fig. 5 (b) : AC output voltage without filtering

Figure 5

Currently, there are only three topologies namely, two-level, three-level, and four-level inverters are employed for UPS applications. The performance of each topology with respect to the key technical parameters is described in the table on next page.

Technical Parameters	Two-level inverter	T-Type Three-Level Inverter (NPC II)	Four-level Inverter
Circuit complexity	Simple	Moderate	Complex control and protection strategies
No of gate driver power supplies required	2 per each leg	4 per each leg	6 per each leg
Semiconductor component cost	Low	Moderate	High
Output filters	Large	Moderate	Small
Overall reliability	High	High	High but questionable due to highly loaded circuit topology
Voltage wave form distortion	Good	Good	Good
DC bus voltage	Low	Medium	High
Voltage stress on DC capacitors/ Number of DC capacitors	More/More	More/Less	Moderate/More
AC input voltage window	Low	Medium	High
Inverter efficiency	97%	98.5%	98.56%
Overall system efficiency	94%	97%	97.1%
MTBF	High	High	Moderate due to a greater number of devices

***Efficiency parameters defined here are considering the 50kVA power capacity, optimized switching frequency of 18 kHZ, and 415 V rated input & output voltage.*

It is understood from the above table that under certain conditions, the four-level inverter efficiency is comparatively bit higher and produces wider voltage window. However on reliability aspect, four-level performance is still unsettled due to its circuit complexity and higher component counts.

Conclusion

Multilevel inverter topologies have been studied to define their performance on availability and energy efficiency for UPS application. Different multilevel inverters were also compared by considering various parameters such as conduction loss, switching loss, filter loss, and number of components. From the above experimental analysis, this technical paper highlights that though five-level topology is a latest advancement yet, but it is not commercially implemented owing to inconclusive performance results: whereas four-level inverter can deliver a bit higher efficiency figure, but its overall circuit complexity and loaded system architecture may cause some challenges on reliability front.

Coming to three-level T-type inverter, it has been there at several sites and tested on reliability parameters for many years. Three-level T-type topology which is an upgraded version of three-level, has been tested to deliver efficiency up to 97% and overall circuit complexity and component counts are also reasonably lesser compared to its latest generation successors.

Certainly, technology advancement should take the front seat moving forward, but replacement should be done after achieving the proven performance at the critical facilities.


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